REMARKS

Claims 1 through 22 are in the application, with Claims 1, 12, 17, 20 and 21 having been amended. Claims 1, 12 and 17 are the independent claims herein. No new matter has been added. Claims 1, 2, 11-13 and 17-22 stand rejected. It is noted with appreciation that claims 3-10 and 14-16 were found to recite allowable subject matter, although objected to as dependent on rejected claims. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC § 102(b)

Claims 1, 2, 11, and 20 are rejected as being anticipated by Yabe, U.S. Patent Application Publication No. 2001/0043123 ("Yabe").

Claim 1, as now clarifyingly amended, is directed to a "ring oscillator" which includes "a plurality of delay cells coupled in series as a ring" and "a replica cell coupled to the delay cells to provide at least one bias signal to the delay cells". Claim 1 further recites that "the replica cell includ[es] a differential transistor pair formed of a first transistor and a second transistor". It is further recited in claim 1 that "the first transistor ha[s] a first terminal and a second terminal coupled to the first terminal, the second transistor ha[s] a first terminal and a second terminal coupled to the first terminal of the second transistor, [and] the first transistor also ha[s] a third terminal and the second transistor also ha[s] a third terminal coupled to the third terminal of the first transistor". The amendment noted above to claim 1 is to the effect that a third terminal of the first transistor is coupled to a third terminal of the second transistor. Support for this amendment is found at FIG. 1 (source terminals 164, 166 and node 162) and page 4, lines 17-20 of the specification.

In rejecting claim 1 as anticipated by Yabe, the Examiner particularly relied upon circuitry shown in FIGS. 6-8 of the reference. As to the first and second transistors recited in claim 1, each having their first and second terminals coupled together, the Examiner relied on diode connected NMOS transistors in variable impedance loads 1a and 2a.

In reviewing FIG. 6 of Yabe, it seems to applicant that the variable impedance loads 1a and 2a correspond in function to active resistors 152, 156 in FIG. 1 of the present application; that transistors Q9 and Q8 in FIG. 6 in Yabe, with their source terminals coupled together, form

a differential pair that corresponds in function to the differential pair formed of transistors 148, 150 in FIG. 1 of the present application; and transistor Q7 in FIG. 6 in Yabe corresponds in function to the current source 160 in FIG. 1 of the present application. It is particularly notable that the gate of Q9 of Yabe's differential pair is coupled to ground, like the prior art arrangement described at page 5, lines 15-22 of the present application, and unlike the arrangement of the replica cell 102 of FIG. 1 of the present application, in which both transistors 148 and 150 have their gates coupled to their drains. Moreover, in applicant's view, it is doubtful that one of ordinary skill in the art would consider that the diode connected transistors in variable impedance loads 1a, 2a of Yabe constitute a "differential pair", since their source terminals are not coupled together.

In any event, and to more sharply distinguish claim 1 from Yabe, it is now specified in claim 1 that the first and second transistors each have a third terminal, and that the two third terminals are coupled to each other. Consequently, it is now believed to be clear that the diode connected transistors in 1a and 2a of Yabe cannot satisfy the first and second transistors as interconnected in accordance with claim 1, since the diode connected transistors in 1a and 2a are not connected to each other. Applicant therefore respectfully requests that the rejection of claim 1 be reconsidered and withdrawn.

Claims 2, 11 and 20 are dependent on claim 1 and are submitted as patentable on the same basis as claim 1.

Claim Rejections – 35 USC § 103(a)

Claims 12, 13 and 21 are rejected as being unpatentable over Yabe.

In regard to this rejection, applicant notes that claim 12 has been clarifyingly amended in the same manner as claim 1, and it is believed that the remarks made above with respect to claim 1 are equally applicable to claim 12. Accordingly, claim 12 is submitted as patentable on the same basis as claim 1, and the same is also the case with respect to claims 13 and 21 which are dependent on claim 12.

Claims 17-19 and 22 are rejected as being unpatentable over Yabe in view of Iravani, U.S. Patent No. 5,936,476 ("Iravani").

Claim 17, as now amended, is directed to a method which includes "providing a ring oscillator that includes a plurality of delay cells and a replica cell coupled to the delay cells to provide at least one bias signal to the delay cells". Claim 17 also specifies that "the replica cell includ[es] a differential transistor pair", "the replica cell and the delay cells each includ[e] active resistors", "each of the active resistors includ[es] a transistor having a gate terminal", "the replica cell also includ[es] an operational amplifier", "the operational amplifier ha[s] an inverting input coupled to a terminal of one of the transistors of the differential transistor pair" and "the operational amplifier ha[s] an output coupled to the gate terminals of the active resistors". Finally, claim 17 also recites the limitation of "applying a reference signal level to a non-inverting input of the operational amplifier to set a common mode output voltage of the ring oscillator".

The newly added limitations that the replica cell and the delay cells include active resistors and that the active resistors each include a transistor having a gate terminal are supported at FIG. 1 (active resistors 126, 130, 152, 156) of the present application, FIG. 2 (transistor 132 with gate terminal 140), and page 3, line 21 to page 4, line 2 of the specification, as well as page 4, lines 10-16 of the specification.

The newly added limitation that the operational amplifier has an output coupled to the gate terminals of the active resistors is supported at FIG. 1 (output 174 of op amp 172) and FIG. 2 and at page 5, lines 1-8 of the specification.

Applicant notes that the output of the amplifier 12 in FIG. 6 of Yabe is not coupled to the active resistors 1a, 2a (1, 2 in the delay cell 10a). Rather, the output of the amplifier 12 controls transistor Q10 (Q6 in the delay cell) to stabilize the level at node N1a (N1 in the delay cell) at the reference level supplied to the inverting input of amplifier 12. It is noted that N1a corresponds to the source terminals of the transistors Q9, Q8 (N1 corresponds to the source terminals of Q3, Q2 in the delay cell), so that the amplifier 12 and its reference input do not set the common mode output voltage of the ring oscillator, inasmuch as the common mode output voltage is at the outputs OUT, OUTn of the delay cell 10a, i.e., at drain terminals of Q2 and Q3.

These defects of Yabe cannot be compensated for by teachings in Iravani, at least because the amplifier 201 (FIG. 3) in Iravani, receives as the non-feedback input a control

voltage VCO_{in} which is the control voltage for the VCO and controls the frequency of oscillation (see column 4, lines 42-43 of Iravani). Thus, the amplifier 201 does not receive a reference signal and does not set the common mode output voltage for the oscillator. On the other hand, as noted before, the amplifier 12 in Yabe receives a reference signal but does not set a common mode output voltage for the oscillator.

It is therefore respectfully submitted that claim 17, at least as now presented, is clearly patentable over the asserted combination of the Yabe and Iravani references. Claims 18 and 19 are dependent on claim 17 and are submitted as patentable on the same basis as claim 17.

CONCLUSION

Accordingly, applicant respectfully requests allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-3460.

Respectfully submitted,

January 25, 2005
Date

Nathaniel Levin
Registration No. 34,860
Buckley, Maschoff & Talwalkar LLC
Five Elm Street
New Canaan, CT 06840
(203) 972-3460